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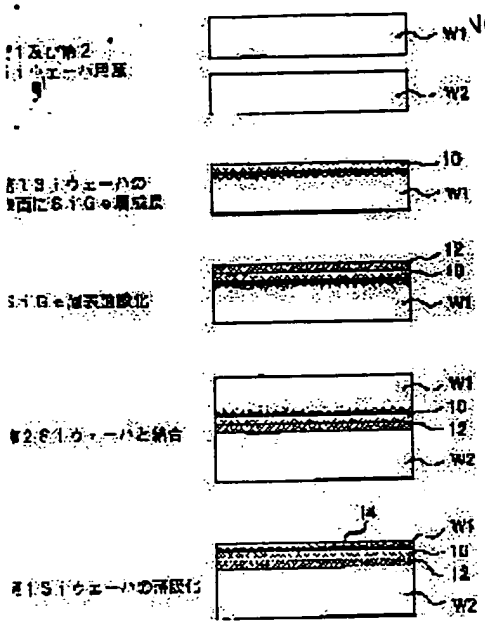

PATENT ABSTRACTS OF JAPAN

(11)Publication number : **2002-164520**

(43)Date of publication of application : **07.06.2002**

(51)Int.Cl. **H01L 27/12**

H01L 21/02

(21)Application number : **2000-358783**

(22)Date of filing : **27.11.2000**

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KIMURA MASAKI

(54) METHOD FOR MANUFACTURING SEMICONDUCTOR WAFER

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a method for manufacturing a semiconductor wafer which can manufacture a semiconductor wafer by a simple manufacturing process which wafer has lattice strain sufficient to improve mobility of electrons in spite of comparatively simple lamination structure and is provided with an Si layer having little crystal defect.

SOLUTION: This method for manufacturing a semiconductor wafer is provided with a process for growing epitaxially an SiGe layer on a surface of a first silicon single crystal wafer, a process for coupling a surface of the SiGe layer with a surface of a second wafer via an oxide film, and a process for thinning the first silicon single crystal wafer coupled with the second wafer and exposing the Si layer including lattice strain.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention relates to the manufacture method of a semiconductor wafer of having the silicon layer which is inherent in grid distortion.
[0002]
[Related Art] As a way method for raising the performance of the semiconductor device using the silicon single crystal, it is effective to raise the degree of electron transfer in a silicon single crystal. Then, the mobility of a carrier is raised and the device which makes high-speed operation possible is examined by by [which are distorted and uses a silicon layer (a distortion Si layer is called hereafter.) for the barrier layer of for example, an n channel MOS transistor] having pulled to the silicon single crystal which has the usual lattice constant (about 5.43A), and having made distortion inherent.
[0003] The manufacture method of a semiconductor wafer of having such a distortion Si layer is indicated by JP,9-180999,A and JP,11-233440,A. Each of such technology is what is distorted by growing Si layer epitaxially and forms Si layer on a SiGe layer with a bigger lattice constant than Si. It was what solves two technical problems of making Si layer generate distortion using the SiGe layer by which grid relief was fully carried out, and not generating transposition, being made and distorted in a SiGe layer, and not making transposition spread at the time of growth of Si layer.
[0004]
[Problem(s) to be Solved by the Invention] However, the two aforementioned methods were not necessarily able to be called simple method with at least 2 times of thin film growth processes (epitaxial growth, spatter, etc.). This is explained in full detail below.
[0005] First, the semiconductor wafer indicated by JP,9-180999,A It is what has the structure of a distortion Si layer / SiGe layer / germanium layer / Si layer / SiO two-layer / Si substrate in order from a wafer front face. the manufacture process As shown in drawing 3 , it is production (Step 100) ->Si layer epitaxial layer (Step 102) ->germanium layer growth (Step 104) ->SiGe layer growth (Step 106) -> grid relief heat treatment (Step 108) -> distortion Si layer growth (Step 110) of a SOI wafer. It was a thing accompanied by four epitaxial growth.
[0006] Moreover, the semiconductor wafer indicated by JP,11-233440,A It is what has the structure of distortion Si layer / CaF two-layer/(SiGe layer) / Si substrate in order from a wafer front face. the manufacture process As shown in drawing 4 , it is deposition (Step 202) ->(SiGe layer growth) (Step 204) -> distortion Si layer growth (Step 206) by the Si wafer preparation (Step 200) ->CaF two-layer spatter. The case here was also what forms a special layer called CaF2 with at least two thin film growth.
[0007] Thus, by the conventional method, since it was what consists of complicated laminated structures accompanied by many processes, the manufacturing cost lacked in versatility highly.
[0008] this invention aims at offering the manufacture method of a semiconductor wafer that the semiconductor wafer which is made in order to solve such a trouble, has sufficient grid distortion to raise the degree of electron transfer in spite of a comparatively simple laminated structure, and has Si layer with few crystal defects can be manufactured according to a simple manufacture process.
[0009]
[Means for Solving the Problem] In order to attain the above-mentioned purpose, the 1st mode of the manufacture method of the semiconductor wafer of this invention The process which grows a SiGe layer epitaxially on the front face of the 1st silicon-single-crystal wafer, it was combined with the process which combines the front face of this SiGe layer, and the front face of the 2nd wafer through an oxide film, and this 2nd wafer -- this -- it is characterized by having the process at which Si layer which thin-film-izes the 1st silicon-single-crystal wafer, and is inherent in grid distortion is exposed
[0010] The 2nd mode of the manufacture method of the semiconductor wafer of this invention The process which grows a SiGe layer epitaxially on the front face of the 1st silicon-single-crystal wafer, The process which forms an oxide film in either [at least] the front face of this SiGe layer, or the front face of the 2nd wafer, The process which pours either [at least] a hydrogen ion or a rare gas ion into the 1st silicon-single-crystal wafer through this SiGe layer, and forms a minute foam layer, this aforementioned oxide film -- minding -- this -- the minute this foam layer after combining the 1st silicon-single-crystal wafer and 2nd wafer -- this -- it is characterized by having the process which exfoliates the 1st silicon-single-crystal wafer

[0011] In the 2nd mode of the above, it is desirable to establish further the process which carries out flattening of the surface of separation of the above-mentioned 1st silicon-single-crystal wafer thin film which exfoliated according to the above-mentioned process which carries out ablation, and moved to the 2nd wafer of the above combining polish, heat treatment, or these. The above-mentioned minute foam layer can be formed in the field which has the grid distortion of the 1st silicon-single-crystal wafer.
[0012] As for the above-mentioned oxide film, in the above 1st and the 2nd mode, it is desirable to be formed in the front face of the above-mentioned SiGe layer of thermal oxidation. As the 2nd wafer of the above, it is desirable to use a silicon-single-crystal wafer.
[0013]
[Embodiments of the Invention] Although the gestalt of operation of this invention is explained using an accompanying drawing below, unless it deviates from the technical thought of this invention, it cannot be overemphasized that various deformation is possible besides the example of illustration.
[0014] (Gestalt of the 1st operation) The manufacture flow of the semiconductor wafer which is the gestalt of operation of the 1st of this invention was shown in drawing 1 . The manufacture flow shown in drawing 1 is only what added the process (b) which grows a SiGe layer to the usual manufacture flow at the time of manufacturing a SOI wafer by the lamination method using the silicon wafer of two sheets fundamentally.
[0015] First, the 1st and 2nd Si wafers W1 and W2 which are finally distorted and serve as material of Si layer are prepared [drawing 1 (a)]. If this Si wafer W1 is single crystal silicon, especially limitation is not carried out but Si wafer produced by the CZ process or the FZ method can be used for it. However, in order to raise the quality of the distortion Si layer which forms a device, it is desirable that a crystal defect uses a few thing near the front face of the wafer used at least. Specifically, the wafer which formed DZ layer near the wafer front face with heat treatment, the wafer which reduced the so-called Grown-in defect in a single crystal by adjusting the raising conditions of a CZ process (or disappearance), FZ wafer, etc. are suitable.
[0016] Next, the SiGe layer 10 is formed in the front face of the Si wafer W1 of the above 1st by epitaxial growth [drawing 1 (b)]. For example, a molecular-beam epitaxial growth system, ultra-high-vacuum chemical-vapor-deposition (UHV-CVD) equipment, etc. can be used for formation of the SiGe layer 10.
[0017] About 10 - 40% of germanium composition of the SiGe layer 10 to form is desirable. The distortion Si layer which has tension distortion sufficient at less than 10% is not formed, but since it will become easy to generate misfit transposition in the SiGe layer 10 according to the difference in the lattice constant of the Si wafer W1 and the SiGe layer 10 if it exceeds 40%, it has a bad influence on the crystallinity of the distortion Si layer finally formed. Moreover, the thickness of the SiGe layer 10 has 10nm - desirable about 1 micrometer. The distortion Si layer which has tension distortion sufficient in less than 10nm is not formed, but if it exceeds 1 micrometer, the device property which is distorted by the increase in a parasitic capacitance etc. and is formed in Si layer will get worse. In addition, even if the SiGe layer 10 from which a lattice constant differs on the 1st Si wafer W1 according to the above-mentioned process is formed, transposition does not occur in the 1st Si wafer W1 side according to the thickness effect of the 1st Si wafer W1.
[0018] Next, an oxide film 12 is formed in the front face of the SiGe layer 10 [drawing 1 (c)]. Formation of an oxide film may use the usual oxidizing [thermally] method, and may deposit it by CVD. if the oxidizing [thermally] method is used -- SiGe layer 10 front face -- chemical -- stable SiO two-layer -- 12 is formed, excessive germanium atom is soon taken out by the SiGe layer 10, and germanium concentration in the SiGe layer 10 becomes high Therefore, even if it is the case where germanium composition at the time of growing epitaxially in order to suppress generating of misfit transposition is made comparatively low, the tension distortion of the distortion Si layer finally formed can be raised by oxidizing thermally SiGe layer 10 front face. Moreover, in order to obtain sufficient tension distortion, thermal oxidation and oxide-film removal may be repeated and may be performed.
[0019] Next, the front face of the oxide film 12 formed in SiGe layer 10 front face and the 2nd Si wafer W2 is stuck, and it heat-treats so that it may become the bond strength which can bear a next thin film-ized process [heat-of-linkage processing and drawing 1 (d)]. Although they will not be limited especially if they are conditions which can bear a next thin film-ized process, when grinding and polish perform thin film-ization, as for heat treatment conditions, it is desirable to carry out at 800-1200 degrees C for about 0.5 to 5 hours.
[0020] Finally the 1st Si wafer W1 is thin-film-ized, it is distorted, and the Si layer 14 is exposed [

drawing 1 (e)]. The thickness of the distortion Si layer 14 has desirable about 1-100nm. Processing is also difficult, when there will be a possibility that the hauling distortion by the SiGe layer 10 may stop being inherent and a good device property will not be obtained in less than 1nm, if it exceeds 100nm.
[0021] The technique to grind can be mentioned after carrying out comparatively for 2 minutes by the wet etching using the acid besides grinding and polish, and the alkaline-water solution as the thin film-ized technique of the Si layer 14, the gas phase etching using plasma, wrapping, or the slice. The heat-of-linkage processing performed before thin-film-izing depending on such thin film-ized technique can be omitted, or it can also join together using adhesives etc.
[0022] (Gestalt of the 2nd operation) The manufacture flow of the semiconductor wafer which is the 2nd operation gestalt of this invention was shown in drawing 2 . The manufacture flow shown in drawing 2 is only what added the process (b) which grows a SiGe layer to the manufacture flow at the time of manufacturing a SOI wafer using the silicon wafer of two sheets by the ion-implantation exfoliating method (called the hydrogen ion exfoliating method and the smart cutting method (registered trademark).) fundamentally. In addition, to the process which oxidizes the front face of the SiGe layer in drawing 2 , since it is the same process as drawing 1 (a) - drawing 1 (c), [drawing 2 (a) - drawing 2 (c)] omit explanation for the second time.
[0023] From the front-face side of the oxide film 12 formed in the front face of the SiGe layer 10, when a hydrogen ion or a rare gas ion pours in on the other hand (drawing 2 (d) hydrogen ion 16) at least through an oxide film 12 and the SiGe layer 10, the minute foam layer 18 is formed into the 1st Si wafer W1 [drawing 2 (d)].
[0024] In order to decide by pouring energy of a hydrogen ion 16 the position (depth) in which the minute foam layer 18 is formed and to generate ablation with next ablation heat treatment bordering on the minute foam layer 18, the pouring dosage (for example, 5x1016-/cm2) exceeding 1x1016-/cm2 is needed. In order to make it Si layer front face on the front face of the maximum of the wafer of the multilayer structure formed by exfoliating certainly have grid distortion (hauling distortion), it is desirable to form the aforementioned minute foam layer 18 in the field (field the front face of the 1st Si wafer W1 to 100nm or less) which has the grid distortion of the 1st Si wafer W1.
[0025] Next, ablation is produced in the aforementioned minute foam layer 18 by sticking the front face of the oxide film 12 formed in SiGe layer 10 front face, and the 2nd Si wafer W2, and adding [drawing 2 (e)] and heat treatment (ablation heat treatment) of 500 degrees C or more [drawing 2 (f)]. Then, you may raise a bond strength by performing heat-of-linkage processing further in an elevated temperature if needed. Moreover, when using this method by recently, without performing ablation heat treatment by exciting the hydrogen ion poured in and pouring in according to the plasma state since the method of exfoliating at a room temperature is also developed although it is a kind of the ion-implantation exfoliating method, ablation heat treatment can be omitted.
[0026] Although the front face of the distortion Si layer 14 after ablation is a mirror plane, since it has some field granularity, flattening of the very few polish of the polish cost called touch polish is performed and carried out [drawing 2 (g)]. It is also possible to carry out flattening combining the technique of carrying out flattening by heat-treating in argon gas or hydrogen gas atmosphere instead of and these. [a touch polish]
[0027] When using the usual resistance heating formula heat treating furnace as heat treatment conditions, 1100-1300 degrees C and heat treatment of about 0.5 - 5 hours are suitable, and when using RTA (Rapid Thermal Annealing) equipment, 1100-1350 degrees C and heat treatment for about 1 - 120 seconds are suitable. Moreover, it can also heat-treat combining these.
[0028] In addition, although the case where an oxide film 12 was formed in the front face of the SiGe layer 10 of the 1st Si wafer W1 was illustrated with the gestalt of operation shown in drawing 1 and drawing 2 , an oxide film may be formed in the 2nd Si wafer W2, and an oxide film may be formed in both the 1st and 2nd Si wafers. Moreover, as 2nd Si wafer W2, when resistivity uses the high resistivity wafer more than 1000-ohmcm, it excels in a RF property and can use as a semiconductor wafer for mobile communications. Furthermore as the 2nd wafer W2, insulating substrates, such as a quartz substrate, silicon on sapphire, SiC, and an alumimium nitride substrate, can also be used.
[0029]
[Example] Although an example is raised to below and this invention is explained to it still more concretely, these examples of it not interpreting in limitation are natural.
[0030] (Example 1 : the gestalt of the 1st operation correspondence) The semiconductor wafer which was shown in drawing 1 and which has sufficient grid distortion on the following conditions according to

the procedure of the gestalt of the 1st operation was manufactured.
[0031] 1. Use Wafer (Preparation of the 1st and 2nd Wafers) [Drawing 1 (a)]
The diameter of 200mm, p type, crystal orientation <100>, 10-ohmcm [0032] 2. Front Face of 1st Wafer -- SiGe Layer Growth (UHV-CVD System) [Drawing 1 (B)]
Material gas: GeH4, Si2H6 growth temperature:700 degree-CSiGe composition:Si0.7germanium0.3 growth thickness:150nm[0033] 3. SiGe Scaling [Drawing 1 (C)]
Oxidization conditions: 800 degrees C, pie ROJIE nick oxidization oxidization thickness:100nm[0034] 4. Joint Process [Drawing 1 (D)]
Both wafers are stuck at a room temperature and they are 1000 degrees C and heat treatment (oxidizing atmosphere) of 2 hours.
[0035] 5. Thin-Film-izing [Drawing 1 (E)]
Surface grinding: It is grinding until the 1st Si wafer ** is set to about 20 micrometers.
Mirror polishing: Grind until the 1st Si wafer ** is set to about 4 micrometers.
It is thin film-ization (technology in which the PACE method was indicated by the No. [2565617] patent) until the 1st Si wafer ** is set to about 100nm by the gas phase etching by the PACE (Plasma Assisted Chemical Etching) method.
[0036] (Example 2 : the gestalt of the 2nd operation correspondence) The semiconductor wafer which was shown in drawing 2 and which has sufficient grid distortion on the following conditions according to the procedure of the gestalt of the 2nd operation was manufactured.
[0037] 1. Use Wafer (Preparation of the 1st and 2nd Wafers) [Drawing 2 (a)]
The diameter of 200mm, p type, crystal orientation <100>, 10-ohmcm [0038] 2. Front Face of 1st Wafer -- SiGe Layer Growth (UHV-CVD System) [Drawing 2 (B)]
Material gas: GeH4, Si2H6 growth temperature:700 degree-CSiGe composition:Si0.85germanium0.15 growth thickness:120nm[0039] 3. SiGe Scaling [Drawing 2 (C)]
Oxidization conditions: 800 degrees C, pie ROJIE nick oxidization oxidization thickness:100nm[0040] 4. Hydrogen Ion Pouring [Drawing 2 (D)]
H+ ion-implantation conditions: 35keV, 8x1016-/cm2 [0041] 5. Ablation Process [Drawing 2 (E) and (F)]
Both wafers are stuck at a room temperature and it exfoliates with 500 degrees C and heat treatment for 30 minutes (nitrogen atmosphere). About 130nm of maximum surface Si layer thickness of the multilayer wafer after ablation.
[0042] 6. 800 Degrees C of Heat-of-Linkage Processings, 2 Hours, Nitrogen Atmosphere [0043] 7. Touch Polish [Drawing 2 (G)]
30nm [0044] of polish cost abbreviation
[Effect of the Invention] As stated above, according to this invention, the effect that the semiconductor wafer which has sufficient grid distortion to raise the degree of electron transfer, and has Si layer with few crystal defects can be manufactured according to a simple manufacture process is attained in spite of a comparatively simple laminated structure.

[Translation done.]

CLAIMS

[Claim(s)]
[Claim 1] it was combined with the process which combines with the front face of the 1st silicon-single-crystal wafer the process which grows a SiGe layer epitaxially, and the front face of this SiGe layer and the front face of the 2nd wafer through an oxide film, and this 2nd wafer -- this -- the manufacture method of the semiconductor wafer characterized by having the process at which Si layer which thin-film-izes the 1st silicon-single-crystal wafer, and is inherent in grid distortion is exposed
[Claim 2] The manufacture method of the semiconductor wafer characterized by providing the following. The process which grows a SiGe layer epitaxially on the front face of the 1st silicon-single-crystal wafer. The process which forms an oxide film in at least the front face of this SiGe layer, or the front face of the 2nd wafer either. The process which pours either [at least] a hydrogen ion or a rare gas ion into the 1st silicon-single-crystal wafer through this SiGe layer, and forms a minute foam layer. this oxide film -- minding -- this -- the minute this foam layer after combining the 1st silicon-single-crystal wafer and 2nd wafer -- this -- the process which exfoliates the 1st silicon-single-crystal wafer
[Claim 3] The manufacture method of the semiconductor wafer indicated by the claim 2 characterized by having the process which carries out flattening of the surface of separation of the aforementioned 1st silicon-single-crystal wafer thin film which exfoliated according to the aforementioned process which carries out ablation, and moved to the 2nd wafer of the above combining polish, heat treatment, or these.
[Claim 4] The manufacture method of the semiconductor wafer indicated by the claim 2 or claim 3 which carries out the feature of forming the aforementioned minute foam layer in the field which has the grid distortion of the silicon-single-crystal wafer of the above 1st.
[Claim 5] The manufacture method of the semiconductor wafer indicated by any 1 term of a claim 1 to the claim 4 characterized by forming the aforementioned oxide film in the front face of the aforementioned SiGe layer by thermal oxidation.
[Claim 6] The manufacture method of the semiconductor wafer indicated by any 1 term of a claim 1 to the claim 5 characterized by using a silicon-single-crystal wafer as the 2nd wafer of the above.

[Translation done.]

TECHNICAL FIELD

[The technical field to which invention belongs] this invention relates to the manufacture method of a semiconductor wafer of having the silicon layer which is inherent in grid distortion.

[Translation done.]

PRIOR ART

[Related Art] As a way method for raising the performance of the semiconductor device using the silicon single crystal, it is effective to raise the degree of electron transfer in a silicon single crystal. Then, the mobility of a carrier is raised and the device which makes high-speed operation possible is examined by by [which are distorted and uses a silicon layer (a distortion Si layer is called hereafter.) for the barrier layer of for example, an n channel MOS transistor] having pulled to the silicon single crystal which has the usual lattice constant (about 5.43A), and having made distortion inherent.
[0003] The manufacture method of a semiconductor wafer of having such a distortion Si layer is indicated by JP,9-180999,A and JP,11-233440,A. On a SiGe layer with a bigger lattice constant than Si, each of such technology is distorted by growing Si layer epitaxially, and forms Si layer. It was what solves two technical problems of making Si layer generate distortion using the SiGe layer by which exists and grid relief was fully carried out, and not generating dislocation, being made and distorted in a SiGe layer, and not making dislocation spread at the time of growth of Si layer.

[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention] As stated above, according to this invention, the effect that the semiconductor wafer which has sufficient grid distortion to raise the degree of electron transfer, and has Si layer with few crystal defects can be manufactured according to a simple manufacture process is attained in spite of a comparatively simple laminated structure.

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, the two aforementioned methods were not necessarily able to be called simple method with at least 2 times of thin film growth processes (epitaxial growth, spatter, etc.). This is explained in full detail below.
[0005] First, the semiconductor wafer indicated by JP,9-180999,A It is what has the structure of a distortion Si layer / SiGe layer / germanium layer / Si layer / SiO two-layer / Si substrate in order from a wafer front face. the manufacture process As shown in drawing 3 , it is production (Step 100) ->Si layer epitaxial layer (Step 102) ->germanium layer growth (Step 104) ->SiGe layer growth (Step 106) -> grid relief heat treatment (Step 108) -> distortion Si layer growth (Step 110) of a SOI wafer. It was a thing accompanied by four epitaxial growth.
[0006] Moreover, the semiconductor wafer indicated by JP,11-233440,A It is what has the structure of distortion Si layer / CaF two-layer/(SiGe layer) / Si substrate in order from a wafer front face. the manufacture process As shown in drawing 4 , it is deposition (Step 202) ->(SiGe layer growth) (Step 204) -> distortion Si layer growth (Step 206) by the Si wafer preparation (Step 200) ->CaF two-layer spatter. The case here was also what forms a special layer called CaF2 with at least two thin film growth.

[0007] Thus, by the conventional method, since it was what consists of complicated laminated structures accompanied by many processes, the manufacturing cost lacked in versatility highly.
[0008] this invention aims at offering the manufacture method of a semiconductor wafer that the semiconductor wafer which is made in order to solve such a trouble, has sufficient grid distortion to raise the degree of electron transfer in spite of a comparatively simple laminated structure, and has Si layer with few crystal defects can be manufactured according to a simple manufacture process.

[Translation done.]

MEANS

[Means for Solving the Problem] In order to attain the above-mentioned purpose, the 1st mode of the manufacture method of the semiconductor wafer of this invention The process which grows a SiGe layer epitaxially on the front face of the 1st silicon-single-crystal wafer, it was combined with the process which combines the front face of this SiGe layer, and the front face of the 2nd wafer through an oxide film, and this 2nd wafer -- this -- it is characterized by having the process at which Si layer which thin-film-izes the 1st silicon-single-crystal wafer, and is inherent in grid distortion is exposed
[0010] The 2nd mode of the manufacture method of the semiconductor wafer of this invention The process which grows a SiGe layer epitaxially on the front face of the 1st silicon-single-crystal wafer, The process which forms an oxide film in either [at least] the front face of this SiGe layer, or the front face of the 2nd wafer, The process which pours either [at least] a hydrogen ion or a rare gas ion into the 1st silicon-single-crystal wafer through this SiGe layer, and forms a minute foam layer, this aforementioned oxide film -- minding -- this -- the minute this foam layer after combining the 1st silicon-single-crystal wafer and 2nd wafer -- this -- it is characterized by having the process which exfoliates the 1st silicon-single-crystal wafer
[0011] In the 2nd mode of the above, it is desirable to establish further the process which carries out flattening of the surface of separation of the above-mentioned 1st silicon-single-crystal wafer thin film which exfoliated according to the above-mentioned process which carries out ablation, and moved to the 2nd wafer of the above combining polish, heat treatment, or these. The above-mentioned minute foam layer can be formed in the field which has the grid distortion of the 1st silicon-single-crystal wafer.
[0012] As for the above-mentioned oxide film, in the above 1st and the 2nd mode, it is desirable to be formed in the front face of the above-mentioned SiGe layer of thermal oxidation. As the 2nd wafer of the above, it is desirable to use a silicon-single-crystal wafer.
[0013]
[Embodiments of the Invention] Although the gestalt of operation of this invention is explained using an accompanying drawing below, unless it deviates from the technical thought of this invention, it cannot be overemphasized that various deformation is possible besides the example of illustration.
[0014] (Gestalt of the 1st operation) The manufacture flow of the semiconductor wafer which is the gestalt of operation of the 1st of this invention was shown in drawing 1 . The manufacture flow shown in drawing 1 is only what added the process (b) which grows a SiGe layer to the usual manufacture flow at the time of manufacturing a SOI wafer by the lamination method using the silicon wafer of two sheets fundamentally.
[0015] First, the 1st and 2nd Si wafers W1 and W2 which are finally distorted and serve as material of Si layer are prepared [drawing 1 (a)]. If this Si wafer W1 is single crystal silicon, especially limitation is not carried out but Si wafer produced by the CZ process or the FZ method can be used for it. However, in order to raise the quality of the distortion Si layer which forms a device, it is desirable that a crystal defect uses a few thing near the front face of the wafer used at least. Specifically, the wafer which formed DZ layer near the wafer front face with heat treatment, the wafer which reduced the so-called Grown-in defect in a single crystal by adjusting the raising conditions of a CZ process (or disappearance), FZ wafer, etc. are suitable.
[0016] Next, the SiGe layer 10 is formed in the front face of the Si wafer W1 of the above 1st by epitaxial growth [drawing 1 (b)]. For example, a molecular-beam epitaxial growth system, ultra-high-vacuum chemical-vapor-deposition (UHV-CVD) equipment, etc. can be used for formation of the SiGe layer 10.

(e)] and heat treatment (ablation heat treatment) of 500 degrees C or more [drawing 2 (f)]. Then, you may raise a bond strength by performing heat-of-linkage processing further in an elevated temperature if needed. Moreover, when using this method by recently, without performing ablation heat treatment by exciting the hydrogen ion poured in and pouring in according to the plasma state since the method of exfoliating at a room temperature is also developed although it is a kind of the ion-implantation exfoliating method, ablation heat treatment can be omitted.
[0026] Although the front face of the distortion Si layer 14 after ablation is a mirror plane, since it has some field granularity, flattening of the very few polish of the polish cost called touch polish is performed and carried out [drawing 2 (g)]. It is also possible to carry out flattening combining the technique of carrying out flattening by heat-treating in argon gas or hydrogen gas atmosphere instead of and these. [a touch polish]
[0027] When using the usual resistance heating formula heat treating furnace as heat treatment conditions, 1100-1300 degrees C and heat treatment of about 0.5 - 5 hours are suitable, and when using RTA (Rapid Thermal Annealing) equipment, 1100-1350 degrees C and heat treatment for about 1 - 120 seconds are suitable. Moreover, it can also heat-treat combining these.
[0028] In addition, although the case where an oxide film 12 was formed in the front face of the SiGe layer 10 of the 1st Si wafer W1 was illustrated with the gestalt of operation shown in drawing 1 and drawing 2 , an oxide film may be formed in the 2nd Si wafer W2, and an oxide film may be formed in both the 1st and 2nd Si wafers. Moreover, as 2nd Si wafer W2, when resistivity uses the high resistivity wafer more than 1000-ohmcm, it excels in a RF property and can use as a semiconductor wafer for mobile communications. Furthermore as the 2nd wafer W2, insulating substrates, such as a quartz substrate, silicon on sapphire, SiC, and an alumimium nitride substrate, can also be used.

[Translation done.]

EXAMPLE

[Example] Although an example is raised to below and this invention is explained to it still more concretely, these examples of it not interpreting in limitation are natural.
[0030] (Example 1 : the gestalt of the 1st operation correspondence) The semiconductor wafer which was shown in drawing 1 and which has sufficient grid distortion on the following conditions according to the procedure of the gestalt of the 1st operation was manufactured.
[0031] 1. Use Wafer (Preparation of the 1st and 2nd Wafers) [Drawing 1 (a)]
The diameter of 200mm, p type, crystal orientation <100>, 10-ohmcm [0032] 2. Front Face of 1st Wafer -- SiGe Layer Growth (UHV-CVD System) [Drawing 1 (B)]
Material gas: GeH4, Si2H6 growth temperature:700 degree-CSiGe composition:Si0.7germanium0.3 growth thickness:150nm[0033] 3. SiGe Scaling [Drawing 1 (C)]
Oxidization conditions: 800 degrees C, pie ROJIE nick oxidization oxidization thickness:100nm[0034] 4. Joint Process [Drawing 1 (D)]
Both wafers are stuck at a room temperature and they are 1000 degrees C and heat treatment (oxidizing atmosphere) of 2 hours.
[0035] 5. Thin-Film-izing [Drawing 1 (E)]
Surface grinding: It is grinding until the 1st Si wafer ** is set to about 20 micrometers.
Mirror polishing: Grind until the 1st Si wafer ** is set to about 4 micrometers.
It is thin film-ization until the 1st Si wafer ** is set to about 100nm by the gas phase etching by the PACE (Plasma Assisted Chemical Etching) method.

[Translation done.]

DESCRIPTION OF DRAWINGS

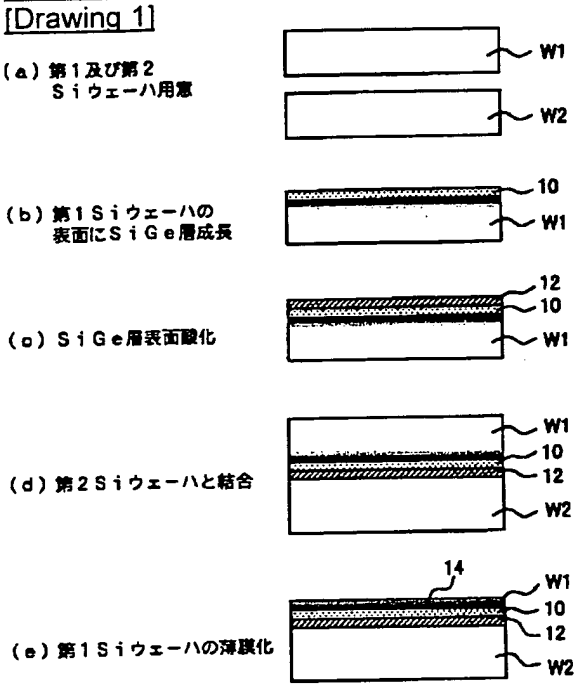
[Brief Description of the Drawings]
[Drawing 1] It is the flow chart which shows the 1st operation gestalt of this invention method.

[Drawing 2] It is the flow chart which shows the 2nd operation gestalt of this invention method.
[Drawing 3] It is the flow chart which shows an example of the manufacture method of the conventional semiconductor wafer.
[Drawing 4] It is the flow chart which shows other examples of the manufacture method of the conventional semiconductor wafer.
[Description of Notations]
10: A SiGe layer, 12:oxide film, a 14:distortion Si layer, 16:hydrogen ion, 18 : a minute foam layer, W1, a W2:Si wafer.

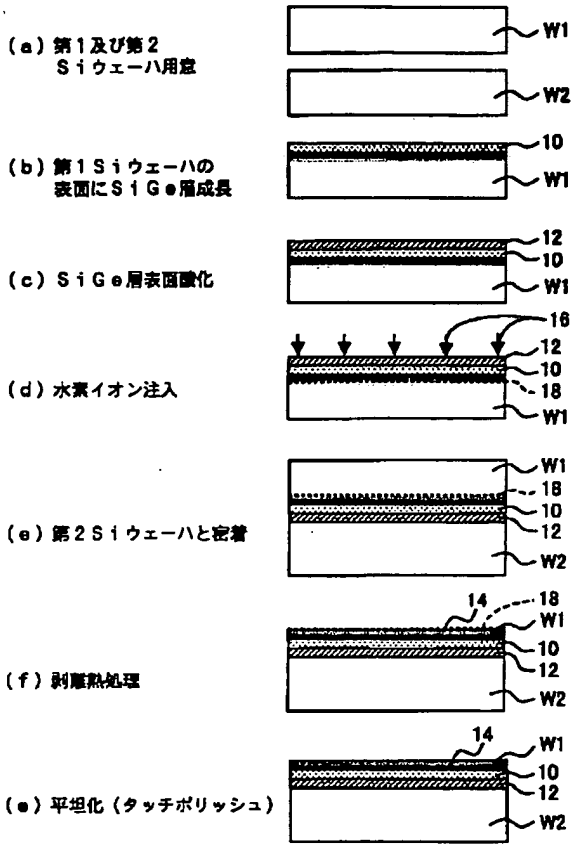
[Translation done.]

DRAWINGS

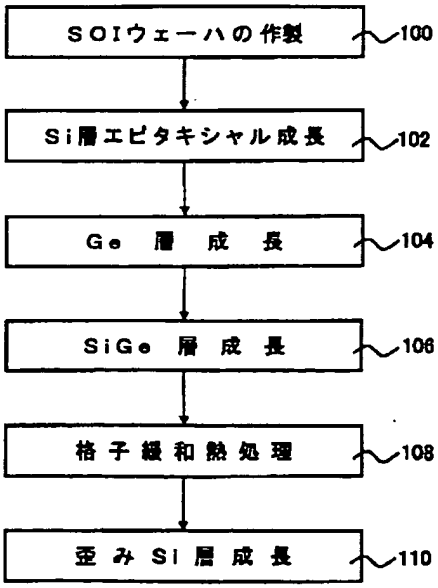
[Drawing 1]



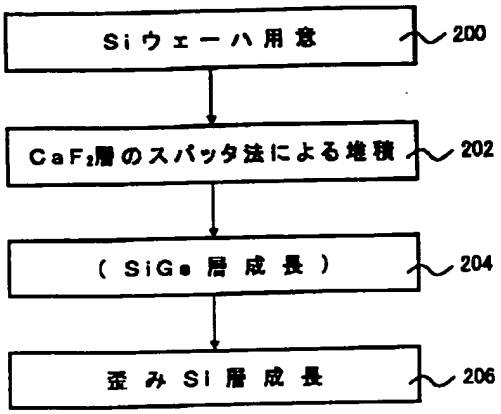
[Drawing 2]



[Drawing 3]



[Drawing 4]



[Translation done.]